

47 GHz VCO With Low Phase Noise Fabricated in a SiGe Bipolar Production Technology

H. Li, *Student Member, IEEE*, H.-M. Rein, *Fellow, IEEE*, R. Kreienkamp, and W. Klein

Abstract—A low-phase-noise and low-cost millimeter-wave voltage-controlled oscillator (VCO) has been fully integrated in commercial SiGe bipolar technologies. By varying the bias voltage of the on-chip varactor, the frequency can be continuously tuned from 43.6 to 47.3 GHz. In this frequency range, single-sideband phase noise between -103 and -108.5 dBc/Hz at 1 MHz offset frequency was measured. The output voltage swing of the differential circuit is about $0.85 V_{p-p}$ for the single-ended and $1.7 V_{p-p}$ for the differential output.

Index Terms—Low-phase-noise VCO, millimeter-wave VCO, SiGe bipolar technology.

I. INTRODUCTION

MILLIMETER-WAVE voltage-controlled oscillators (VCOs) are key components in advanced communication and sensor systems. Potential applications which require oscillation frequencies around 40 GHz are optical-fiber TDM (time-division multiplexing) systems with data rates of 40 and 80 Gbit/s, respectively, and automotive radar systems (possibly in conjunction with a frequency doubler). Here, LC oscillators are preferred to other approaches due to their lower phase noise. 38 GHz and 62 GHz monolithically integrated VCOs with low phase noise (but with comparatively small tuning range) have been presented which were fabricated in laboratory InP-based HBT technologies [1], [2]. However, to the best of the authors knowledge no 40 GHz VCO with low phase noise, wide frequency tuning range and high output power has been monolithically integrated (i.e., including the resonant circuit) in a commercial SiGe bipolar technology. Therefore, we designed several VCOs which were fabricated in Infineon's production technology B7HF. One of them shall be presented here.

II. CIRCUIT CONCEPT AND DESIGN

The circuit diagram is shown in Fig. 1. A fully differential configuration was chosen because of the following advantages (compared to an unsymmetrical configuration).

- It simplifies clock generation in multi-Gbit/s optical-fiber systems due to the differential clock input of the driven circuits.
- On-chip noise problems are substantially reduced.
- High-frequency grounding as well as on- and off-chip decoupling of supply and bias voltages are less critical due to

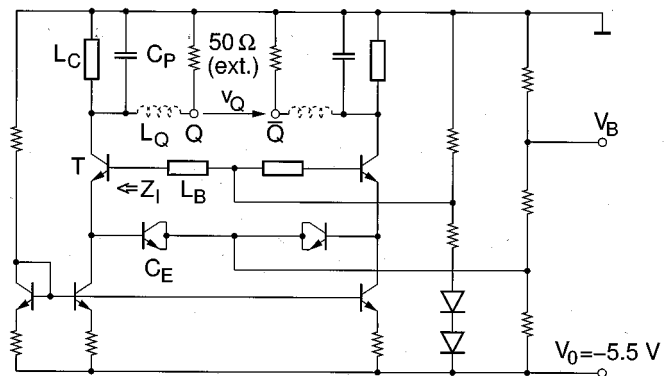


Fig. 1. Circuit diagram of the differential VCO. Apart from the 50Ω external load and (potentially) the bond inductance L_Q , the complete circuit is integrated on the chip. L_B and L_C are microstrip lines.

the virtual ground nodes. Thus, e.g., mounting and packaging are simplified.

- The virtual ground nodes allow to realize easily adjustable on-chip inductances (see below) and thus to use the same IC for different applications in a wide frequency range.

In the circuit of Fig. 1, the principle of a negative-resistance oscillator is applied. The impedance Z_I between the base of transistor T and virtual ground shows a negative real part and a capacitive reactance, both influenced by the varactor C_E . This varactor, which allows to tune the oscillation frequency by varying the bias voltage V_B (e.g., via an external potentiometer), is realized by the shunted base-emitter and base-collector junctions of a transistor. The required inductive reactance at the base is realized by a short microstrip line L_B , with the signal line in the third and the ground plane in the first metallization layer. The characteristic impedance is about 50Ω . Another microstrip line with inductive behavior, L_C , optimizes the load impedance at the collector node of T , mainly with respect to maximum output power. Besides L_C , this load is given by the bond pad capacitance C_P , the external 50Ω load, and—if the chip is mounted—by the bond inductance L_Q .

In order to demonstrate reliable operation in a wide frequency range and to avoid redesigns if the oscillator shall be used for different applications, the lengths of L_B and L_C are adjustable within a wide range¹. This can easily be done by cutting shorting bars in the upper metallization layer between the two complementary lines of a differential microstrip line, e.g., by using an ultrasonic cutter (of course, for higher-volume production this line adjustment should be performed via the final metallization mask). The shorting bars for the lines L_B and L_C are visible

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H. Li, H.-M. Rein, and R. Kreienkamp are with Ruhr-University Bochum, Bochum, Germany (e-mail: rein@aghl.ruhr-uni-bochum.de).

W. Klein is with Infineon Technologies, Munich, Germany.

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¹Sometimes, adjusting L_B and L_C can also be helpful to compensate for potential design inaccuracy or fabrication spread.

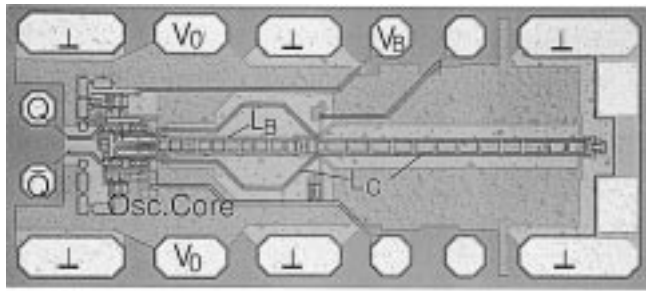


Fig. 2. Chip photo of the VCO (0.4 mm \times 0.9 mm).

in the chip photograph of Fig. 2. It should be noted that for operation near the oscillator's upper frequency range (presented below) the long scratchable part of line L_C in the right half of the chip is not required so that the chip area could be reduced considerably. The distance between the shorting bars was chosen in such a manner that—in combination with the varactor—the oscillation frequency can be continuously adjusted within the total range of interest depending on the applications, here between about 35 and 48 GHz.

The oscillator was designed by ac and transient simulations with a modified version of SPICE 3 and by harmonic balance simulations with SERENADE/Ansoft (especially for minimizing phase noise). In the operating point, a collector current of 15 mA flows through each transistor T . The transistor size proved to be optimal if designed for the maximum admissible collector current density. The characteristic impedances and the required lengths of the microstrip lines were roughly calculated by use of classical transmission line equations. These results were checked by the more accurate computer programs FastHenry [3] and FastCap [4], which additionally allow to calculate the line losses at high frequencies.

III. EXPERIMENTAL RESULTS

The circuit was fabricated in the SiGe bipolar production technology of Infineon, B7HF. It is a self-aligned double-polysilicon technology with a gradient of the Ge concentration in the epitaxial base. The transit frequency f_T and the maximum oscillation frequency f_{max} are both between 70 and 75 GHz. For cost reduction, the present design was restricted to three (Al) metallization layers with a thickness of 2.8 μm for the upper layer and 0.4 μm for the lower layer. From simulations, improved circuit performance is expected if the maximum of four layers is used.

The circuit in Fig. 1 was measured mainly on wafer using RF probes and a 50 GHz spectrum analyzer. For the differential output signal a ground-signal-signal-ground (GSSG) probe was used. On-wafer measurements, which are usual practice in nearly all publications on millimeter-wave oscillators, are justified here, since for the intended applications, the oscillator will probably drive a circuit which is located on the same chip. As another solution, a multichip module is also taken into consideration. This means that the two output pads of the oscillator chip are directly bonded to the input pads of the driven chip. To check the behavior of the oscillator in this environment, the chip was mounted on a measuring socket with copper-clad teflon substrate using conventional wire bonding [5]. In this case, the RF

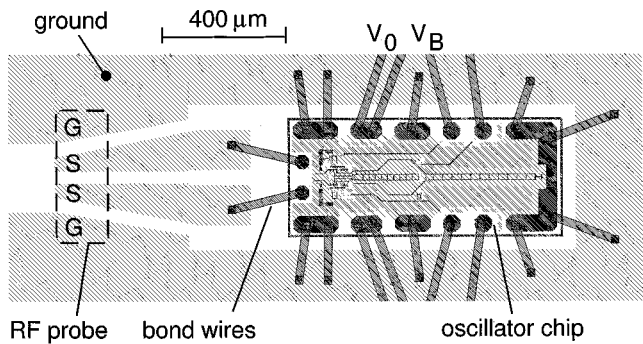


Fig. 3. Schematic section of the measurement substrate with the mounted chip. The hatched areas of the teflon substrate represent the upper copper layer.

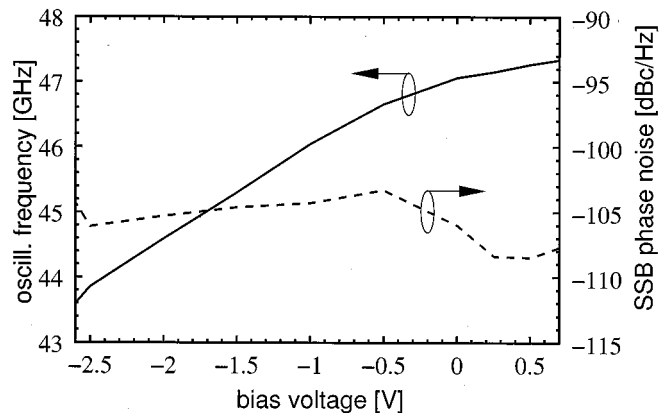


Fig. 4. Measured oscillation frequency and SSB phase noise in dependence on bias voltage V_B .

probe was placed near the ends of two elongated pads of the teflon substrate which are connected to the output pads of the oscillator chip by bond wires (see Fig. 3).

The measuring results of oscillator chips mounted in this way differ only slightly from on-wafer measurements. This experience was confirmed by simulations which especially show only a small influence of the bond inductances (about 0.2 nH) and the bond pad capacitances (about 25 fF) of the measurement socket used here. Therefore, the experimental results presented now can be restricted to on-wafer measurements. These results are obtained with the first technological run and without any redesign. As shown in Fig. 4, the oscillation frequency can continuously be tuned from 43.6 to 47.3 GHz (i.e., by about 8%), if the corresponding bias voltage V_B (see Fig. 1) is varied from -2.6 to $+0.7$. In this frequency range, the single-sideband (SSB) phase noise varies between -103 and -108.5 dBc/Hz at 1 MHz offset from the carrier (see Fig. 4). This low phase noise is comparable to that presented in [1] (-108 dBc/Hz) despite the much wider tuning range of our oscillator. The differential output voltage swing is quite high and changes between 1.6 and 1.8 V_{p-p} for 50 Ω loading of each node (not shown in Fig. 4). This corresponds to an output power of about 5.6 dBm for the differential and 2.6 dBm for the single-ended output, respectively. The spectrum of the (uncorrected) single-ended output power at a center frequency of about 45 GHz is shown in Fig. 5. The total power consumption of the oscillator is 280 mW at a supply voltage of $V_0 = -5.5$ V.

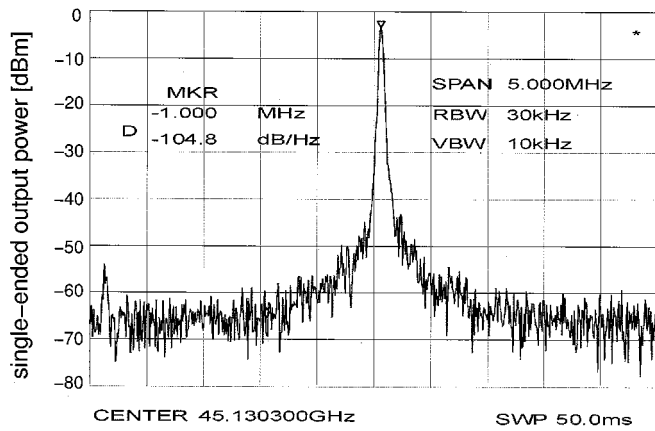


Fig. 5. Measured single-ended output power spectrum at a center frequency of 45.1303 GHz (0.5 MHz per division). Due to the losses of the coaxial measurement cable, 5 dBm must be added to this plot to obtain the real output power.

IV. CONCLUSION

It has been demonstrated that low-cost VCOs for frequencies above 40 GHz can be realized in a commercial SiGe production technology. To the best of the authors knowledge, the high oscillation frequency and low phase noise at wide tuning range presented in this paper have not yet been published for

fully integrated oscillators in Si-based technologies. Since millimeter-wave frequency dividers have been developed in the same technology [6], powerful phase-locked loops can be built at low costs.

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